	L #	Hits	Search Text	DBs	Time Stamp
1	L1	15389	(bitline or bit adj line) and oxide and storage	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/25 14:56
2	L2	1207	sacrificial and 1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/25 14:56
3	L3	561	doped adj polysilicon and 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/25 14:56
4	L4	144	strip and 3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/05/25 14:56

	L #	Hits	Search Text	DBs	Time Stamp
5	L7	6	(("6566219") or ("6168992") or ("6063658")).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/25 15:44
6	L8	11	("4651184" | "4833516" | "4890145" | "5034787" | "5064777" | "5156992" | "5198383" | "5223447" | "5360758" | "5563085" | "5614431").PN.	US-PGPUB; USPAT; USOCR	2005/05/25 15:47
7	L9	11	("6063658").URPN.	USPAT	2005/05/25 15:47

US-PAT-NO: **6063658**

DOCUMENT-IDENTIFIER: US 6063658 A

TITLE: Methods of making a trench **storage** DRAM cell including a step transfer device

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US Patent No. - PN (1):
6063658

TITLE - TI (1):
Methods of making a trench **storage** DRAM cell including a step transfer device

Brief Summary Text - BSTX (5):
Large DRAMs are silicon based. Each DRAM cell typically includes a single MOS field effect transistor, a charge transfer device, with one of its source/drain diffusions connected to a **storage** capacitor. The other of the source/drain diffusions of the MOSFET typically is connected to a **bit line**. The gate typically is connected to a word line.

Drawing Description Text - DRTX (6):
FIG. 16 represents an overhead view of the embodiment of a DRAM cell according to the present invention shown in FIG. 8 including a folded **bit line**;

Drawing Description Text - DRTX (7):
FIG. 17 represents an overhead view of the embodiment of a DRAM cell according to the present invention shown in FIG. 8 including an open **bit line**; and

Detailed Description Text - DETX (4):
FIG. 1 shows a known Merged Isolation and Node Trench cell (MINT) including a planar transfer device. The device shown in FIG. 1 includes a deep trench capacitor 1, a shallow trench isolation region 2, a **bit line** contact

3, a word line 5, or transfer device gate, gate **oxide** 7, and n+ source/drain regions 9 and 11. Buried strap 12 connects the deep trench capacitor **storage** node 1 to the source/drain diffusion 11 of the transfer device.

Detailed Description Text - DETX (6):
The embodiment of the DRAM cell according to the present invention, shown in FIG. 2, includes deep trench capacitor 13, isolation region 15, transfer device gate 17, buried strap 19, gate **oxide** 21, n+ diffusion area 23, and **bit line** contact 25. As can be seen in FIG. 2, the isolation region 15 is formed at least partially over the deep trench capacitor 13. Additionally, the gate **oxide** 21 is formed in an "L" shape.

Detailed Description Text - DETX (10):
The embodiment of the present invention shown in FIG. 8 includes deep trench capacitor 27 with node dielectric 25 formed on the side wall. N+ regions 29 and 31 may be formed in the substrate adjacent a deep trench capacitor for the buried **storage** plate. Above n+ region 29 and 31 in the substrate may be arranged p doped regions 33 and 35.

Detailed Description Text - DETX (11):
Arranged around the boundary of the upper portion of the deep trench capacitor and the substrate may be a collar **oxide** 37. The collar **oxide** 37 may be formed to suppress the parasitic device leakage between the buried plate 29, 31 and the buried strap 45. The deep trench itself may be filled with n+ doped polycrystalline silicon.

Detailed Description Text - DETX (13):
Three sides of the transfer device gate 41 may abut isolation region 39. The transfer device gate 41 may be made of n+ polycrystalline silicon. A layer of gate **oxide** 43 may be arranged at the boundary between the transfer device gate 41 and the p type substrate region 35.

Detailed Description Text - DETX (14):

As in the embodiment shown in FIG. 2, the embodiment shown in FIG. 8 may include an L-shaped gate **oxide** 43. The corner of L-shaped gate **oxide** 43 may be rounded or square. The embodiment of the DRAM cell according to the present invention shown in FIG. 8 may also include a buried n+ diffusion strap 45 connecting the **storage** node located inside of deep trench capacitor 27 to the source/drain diffusion of transfer device 46. Such strap is typical of known trench DRAM cells that include a self-aligned buried strap (BEST). For example, see Nesbit et al., A 0.6 .mu.m.sup.2 256 Mb Trench DRAM Cell With Self-Aligned BuriEd STrap (BEST), IEEE (1993), the entire contents of which are hereby incorporated by reference.

Detailed Description Text - DETX (15):

The buried n+ diffusion strap 45 may be formed under the transfer device gate 41. The other source/drain diffusion region, **bitline** diffusion 47, of transfer device 46 may be located adjacent the transfer device gate 41. The transfer device gate may be connected to word line conductor as shown in FIG. 16 through word line contacts 50 (active word line) and 52 (passing word line) formed in **oxide** 59 and nitride 57 above transfer device gate 41.

Detailed Description Text - DETX (17):

A **bit line** contact 49 may connect the source/drain diffusion 47 of the transfer device 46 to the **bit line** 63 running over dielectric layer 67. The **bit line** contact may be provided over the n+ diffusion region 47. Nitride spacers 51, 53 and nitride layers 57, 61 may be provided to form a **bit line** contact 49 borderless to transfer device gate 41.

Detailed Description Text - DETX (18):

FIG. 16 illustrates an overhead view of a memory cell according to the present invention. In the embodiment shown in FIG. 16, the wordline

conductor
may be formed using a sub-lithographic patterned technique, such as spacer
wordline or hybrid resist photolithography to produce the folded **bit line** cell.
Alternatively, utilizing the embodiment of the memory cell shown in FIG. 8, an
open **bit line** cell, as shown in FIG. 17, may also be built with a word line
defined by a normal lithographic technique.

Detailed Description Text - DETX (20):
The embodiment shown in FIGS. 15 and 18 includes gates 73. The gates may be
made of n+ poly silicon. Gate **oxide** 71 may be provided adjacent a side between
gates 73 and substrate 77 and the bottom surface of gates 73 between gates 73
and substrate 77. Gate isolation insulators 72 may be provided between gates
73 on the side of the gates opposite gate **oxide** 71. The gate isolation
insulator 72 may be made of nitride and be self-aligned to the deep trench
capacitor.

Detailed Description Text - DETX (21):
Extending above gates 73 as shown in FIG. 15 may be word line conductors 74.
Word line conductors 74 may be made of W or WSi.sub.x. The space between word
lines 74 and the space between word lines and **bit line** contact 80 may be filled
by insulating material 82. Any suitable insulating material may be used as the
insulating material 82.

Detailed Description Text - DETX (23):
In regions between gates 73, n+ diffusions 75 may be formed on the substrate
77. The substrate may be a typical p-type silicon substrate. Nitride spacers
76 may be arranged adjacent gate isolation insulators 72 and over a portion of
gates 73. Nitride spacers 76 may also extend at least partially on top of n+
diffusions 75. There may be a thin layer of **oxide** between spacers 76 and the
top surface of n+ diffusions 75.

Detailed Description Text - DETX (24):
Bit line contact 80 may be formed over n+ diffusion 75 for providing connection between a **bit line** 81, n+ diffusion, and, ultimately, the DRAM cell.

Detailed Description Text - DETX (25):
The embodiment of the memory cell shown in FIG. 15 according to the present invention may also include n+ buried strap 78. Such strap is typical of known trench DRAM cells that include a self-aligned buried strap (BEST). For example, see Nesbit et al., A 0.6 .mu.m.sup.2 256 Mb Trench DRAM Cell With Self-Aligned BuriEd STrap (BEST), IEEE (1993). Buried strap 78 may be arranged under a portion of gate 73 and underlying gate **oxide** layer 71. Additionally, buried strap 78 may extend downwardly as shown in FIG. 15 to contact collar **oxide** 84 surrounding the deep trench as described below in greater detail.

Detailed Description Text - DETX (26):
As shown in FIG. 15, this embodiment of the DRAM cell according to the present invention may include n+ buried **storage** node plate 79. The n+ buried **storage** node plate may be formed in the substrate 77 adjacent sides of the deep trenches.

Detailed Description Text - DETX (27):
As stated above, buried plate may be formed adjacent sides of the deep trenches. The deep trenches include n+ poly silicon fill 85. Collar **oxide** 84 may surround the n+ poly silicon fill 85. In the embodiment shown in FIG. 15, collar **oxide** 84 extends from above the deepest extent of n+ buried strap 78 to below the top of the buried plate 79.

Detailed Description Text - DETX (28):
The DRAM cell shown in FIG. 15 may include node dielectric 86 surrounding the n+ poly silicon fill 85. The node dielectric may be arranged between n+ polycrystalline silicon fill and the substrate 77, below collar **oxide**

the spacers of a corresponding size may be utilized to automatically create the correct positioning of the deep trench relative to the above-referenced structures, making the other structures self-aligning.

Detailed Description Text - DETX (43):

The surface of the deep trench, spacers, and other exposed surfaces may then be covered by CVD **oxide** and CVD nitride. The composite **oxide** and nitride liner 129 may be used as a doping mask during formation of the buried plate 79. The resulting structure is shown in FIG. 4.

Detailed Description Text - DETX (45):

After completing etching of the deep trench, n+ buried capacitor plates 130 and 132 may be formed in the substrate. The buried capacitor plates may be formed by filling the deep trench 136 with arsenic doped glass (ASG) and diffusing arsenic into the substrate from the trench walls not covered by the **oxide**/nitride liner 129. Node dielectric may then be formed after removing the ASG.

Detailed Description Text - DETX (46):

The deep trench 136 may then be filled with a first layer of n+ doped polycrystalline silicon. The polycrystalline silicon may be recessed to a first level. Next, collar **oxide** 134 may be deposited and etched.

Detailed Description Text - DETX (47):

A second layer of n+ **doped polysilicon** may be deposited over the first layer of n+ polysilicon and recessed to a second level below the **oxide** spacer 124 around the oversized trench top. A portion of the exposed collar **oxide** and node dielectric may then be removed, creating an opening for the buried strap 142. Thin damage preventing layer 129 may also be removed during the node dielectric **strip**.

Detailed Description Text - DETX (50):

After **oxide** 124, 116 nitride 122 and **oxide** 120 are stripped,

sacrificial
oxide may be grown over the exposed silicon substrate and polycrystalline silicon surface. The **sacrificial oxide** may then be etched. This is to remove any silicon surface damage before growing the gate **oxide**. If necessary, a device channel region may be implanted before removing the **sacrificial oxide**.

Detailed Description Text - DETX (51):
After stripping the **sacrificial oxide,** gate **oxide** 143 may be grown over the exposed substrate, which typically is silicon. Thicker **oxide** may be grown over the doped polycrystalline silicon 136 during the gate oxidation.

Detailed Description Text - DETX (52):
After gate **oxide** 143 formation, the open area over the deep trench may be filled with n+ doped polycrystalline silicon. The upper surface of the device may be planarized. The polysilicon may then be recessed. Any recess created may then be filled with SiO.sub.2 139. SiO.sub.2 deposited in the recess may be deposited by chemical vapor deposition (CVD). After deposition, the SiO.sub.2 may be planarized. The resulting structure is shown in FIG. 6.

Detailed Description Text - DETX (54):
As shown in FIG. 7, the isolation region 140 may, at least partially, overlap deep trench 136. Preferably, the isolation region extends deeper into the substrate than buried diffusion strap 142. The buried diffusion strap 142 is formed by out-diffusion of n-type dopant from trench fill polycrystalline silicon 136 during the gate **oxide** formation and STI process. By forming the isolation region so that it extends deeper into the substrate than the buried diffusion strap may help to isolate the buried strap in one cell from the buried strap in the adjacent cell. The buried strap n+ diffusion becomes the source/drain diffusion of the transfer device 145. After planarization of the

the **oxide**
spacer 162. The exposed collar **oxide** and node dielectric may then be removed,
creating an opening for the buried strap 142. A third layer of polycrystalline
silicon may then be deposited and recessed to the level shown in FIG. 14. N+
dopant may be diffused out of the opening by thermal cycles during the
subsequent process steps to form a buried strap.

Detailed Description Text - DETX (71):
The next step in the process involves forming the transfer device gate.
After **oxide** spacers 162 are removed, **sacrificial oxide** may be grown over the
exposed silicon substrate and polycrystalline silicon surface and may then be
etched. This is to remove any silicon surface damage before growing gate
oxide.

Detailed Description Text - DETX (72):
If necessary, device channel region may be implanted before removing the
sacrificial oxide. After stripping **sacrificial oxide,** gate **oxide** 71 may be
grown over the exposed silicon substrate. Thicker **oxide** may be grown over the
exposed doped polycrystalline silicon during the gate oxidation.

Detailed Description Text - DETX (73):
After gate **oxide** 71 formation, the open area over the deep trench may be
filled with n+ doped polycrystalline silicon. The upper surface of the device
may be planarized. The polysilicon may then be recessed. Nitride may then be
deposited and etched to form spacers 76, shown in FIG. 15, around the perimeter
of the polysilicon gate opening.

Detailed Description Text - DETX (74):
After formation of word line contact, word line, **bit line** contact and **bit**
line may be formed, in a manner similar to that described above.

Claims Text - CLTX (10):
depositing **oxide** in the opening; and